ABSTRACT

[1106] A direct downconversion receiver architecture having a DC loop to remove DC offset from the signal components, a digital variable gain amplifier (DVGA) to provide a range of gains, an automatic gain control (AGC) loop to provide gain control for the DVGA and RF/analog circuitry, and a serial bus interface (SBI) unit to provide controls for the RF/analog circuitry via a serial bus. The DVGA may be advantageously designed and located as described herein. The operating mode of the VGA loop may be selected based on the operating mode of the DC loop, since these two loops interact with one another. The duration of time the DC loop is operated in an acquisition mode may be selected to be inversely proportional to the DC loop bandwidth in the acquisition mode. The controls for some or all of the RF/analog circuitry may be provided via the serial bus.